**WEEK4 PROGRAM**

**REGISTER FILE**

**Students have to complete reg\_file.v**

Step1) **iverilog -o testreg lib.v reg\_file.v tb\_reg\_file.v**

If the compilation went OK, you won't see any output. What this does is create a file called testreg that we can feed to the simulator.

Step2) **vvp testreg**

You can observe output on the console

Step3) **gtkwave tb\_reg\_file.vcd**

Output waveform will be observed.